CLAIM AMENDMENTS

Please cancel claims 1-8 and 14-17 without prejudice or disclaimer

Claims 1-8. (Canceled).

9. (Original) An integrated circuit (IC), comprising:

a cascoded n-channel differential amplifier with current source loads, wherein the differential amplifier comprises thin oxide transistors; and

a common source amplifier coupled to the differential amplifier, wherein the common source amplifier comprises a thick oxide transistor, wherein the common source amplifier biases the differential amplifier.

10. (Original) The IC of claim 9, wherein the first common source amplifier provides a gain.

11. (Original) The IC of claim 9, wherein the differential amplifier comprises a current source coupled to a first transistor, wherein a source of the first transistor is coupled to a drain of a second transistor, wherein a source of the second transistor is coupled to a drain of a third transistor, wherein a source of the third transistor is coupled to a ground, wherein a gate of the thick oxide transistor is coupled to a drain of the first transistor.

12. (Original) The IC of claim 11, wherein a threshold voltage of the thick oxide transistor allows a gate to source voltage of the thick oxide transistor to keep the drain of the first transistor in a saturation region.

13. (Original) The IC of claim 9, further comprising:

a circuit coupled to the differential amplifier to provide common mode feedback.

Claims 14-17. (Canceled)

18. (Original) A method comprising:

generating a first gain through a first circuit having stacked transistors of a first oxide thickness;

generating a second gain through a second circuit having transistors of a second oxide thickness, wherein the second oxide thickness is greater than the first oxide thickness, wherein the second circuit is coupled to the first circuit, wherein the second circuit provides DC coupling between the first circuit and the second circuit, wherein the second circuit has a lower power supply than the first circuit.

19. (Original) The method of claim 18, further comprising:

generating a common mode output voltage.

20. (Original) The method of claim 19, further comprising:

providing a negative feedback to the first circuit.

21. (Original) The method of claim 20, further comprising:

reducing the common mode output voltage if the common mode output voltage rises above a reference voltage.